SOLUTION BRIEF

5G User Plane Function (UPF) – Performance with ASTRI

Describes a multi Terabit solution using Intel® Architecture technology to implement 5G UPF

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Executive Summary

One of the challenges faced by network operators is how to provide a fast, latency-sensitive, and cost-effective gateway function between the edge and the data network, especially as mobile network traffic continues to multiply. With the onset of broad commercial deployment of 5G networks, network traffic compound annual growth rate (CAGR) is set to increase even further. Early data from live 5G launches suggests that typical 5G user equipment (UE) consumes 3x more data than its 4G counterpart.

This Solution Brief articulates the performance benefits for 5G with ASTRI 5G Core User Plane Function (UPF), 2nd generation Intel® Xeon® Scalable processors, and Intel® Ethernet Controller 800 Series.

This document is part of the Network Transformation Experience Kit, which is available at https://networkbuilders.intel.com/network-technologies/network-transformation-exp-kits.

Introduction

The architecture of 2nd generation Intel® Xeon® Scalable processors (formerly codenamed Cascade Lake) provides a multitude of benefits for users who wish to take advantage of Network Functions Virtualization (NFV) architecture and also provide high speed performance for packet forwarding functionality such as User Plane Function (UPF).

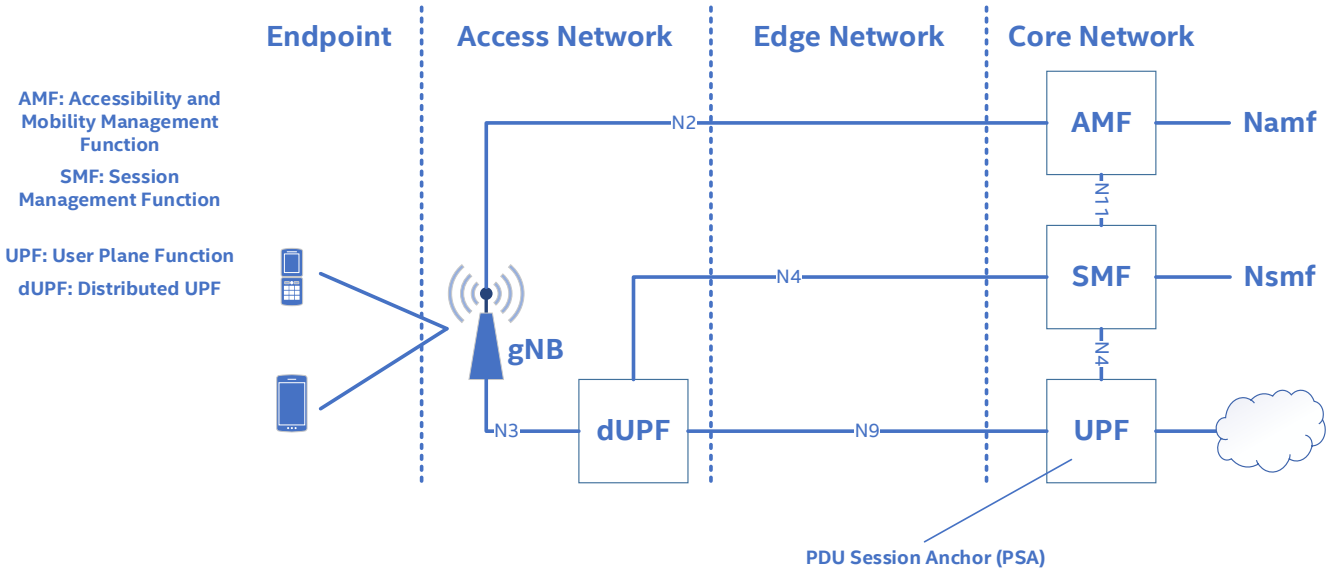
As speeds evolve in the 5G network, operators must enable additional services in a cost-sensitive environment, while delivering infrastructure capability to address this traffic growth at reduced cost-per-bit. The feature-rich Intel® Xeon® processor architecture allows customers to meet network throughput requirements, while also allowing applications to be portable and scalable. In addition, Intel® Ethernet Controller 800 Series (formerly Columbiaville) provides 100G network connectivity functionality to fully utilize the Intel® Xeon® processor cores.

With the introduction of Control and User Plane Separation (CUPS) for Evolved Packet Core (EPC) functions in the 3GPP Release v14, operators can gain incremental control over the management of data packets in the network and provide additional services at the network edge. Also, 5G compels a greater focus on lower latency and greater number of devices, as well as increased bandwidth for users in the network. These are critical differentiators for network operators and are driving forces in the move to a more dense and faster 5G UPF architecture.

Separating the control plane from the user plane allows operators to provide a more flexible and real-time network. Operators can also address the demand for greater control in how applications are deployed. In the solution described in this document, the ASTRI UPF was used to demonstrate a typical example of User Plane Function of mobile broadband use cases. The ASTRI 5G Core UPF delivers high network throughput and can leverage the Dynamic Device Personalization (DDP) capability on Intel® Ethernet Controller 800 Series to achieve fine-grain load balancing and take advantage of certain offload capabilities. These capabilities can be distributed close to the user to enable low latency and time-sensitive usage scenarios, as well as providing the flexibility to be deployed in either a distributed or centralized manner.

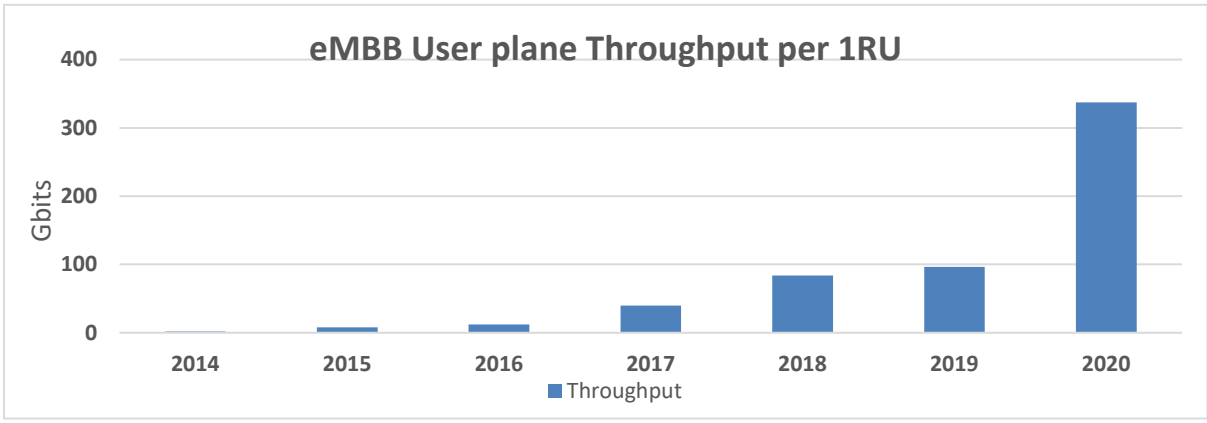
The UPF provides the following:

- The interconnect point between the mobile infrastructure and the Data Network (GTP-U).
- The Protocol Data Unit (PDU) session anchor point for providing mobility within and between Radio Access Technologies (RATs)
- Packet routing and forwarding (DPI, NAT, Security, Service Chaining, Policy Enforcement, Breakout)
- Application detection using Service Data Flow (SDF) traffic filter templates
- Per-flow QoS handling
- Traffic usage reporting for billing and the Lawful Intercept (LI) collector interface



Solution Description

As shown in the diagram below, traffic throughput per Radio Unit (RU) is increasing yearly. To keep pace with the rapid increase in data, Intel has demonstrated a number of optimizations in the UPF workload, enabled by 2nd generation Intel® Xeon® Scalable processors, the Intel 800 Series Controller, and software technologies (DDP and Data Plane Development Kit) to allow customers to service this demand in a scalable and cost-effective manner. One of the key metrics for delivering gateway infrastructure is ensuring that throughput-per-dollar is highly optimized.



The solution demonstrates the functionality of the UPF on Intel® Architecture using 2nd generation Intel® Xeon® Scalable processors (formerly codenamed Cascade Lake) and Intel® Ethernet Controller 800 Series (formerly codenamed Columbiaville) in a virtualized and cloud native environment. The demo is based on the ASTRI software stack, demonstrating over 1.3Tbps of traffic with containerized, VPP-based UPF, orchestrated with Kubernetes (K8s).

Below are the details of the solution demonstrated by Intel with the ASTRI UPF:

- Generating live 5G user plane traffic for 1 million subscribers
- Measuring throughput and latency through:
  - Cloud Native infrastructure
  - Optimized for 5G Core application
- Market-leading performance on commodity hardware:
  - Greater than 1.3Tbps of network traffic in 4U footprint using cost-efficient 2nd generation Intel® Xeon® Scalable 6230N processor (20 core)
  - Using Intel® Ethernet 800 Controller Series 100G adapters
  - Software optimized libraries (Data Plane Development Kit, Vector Packet Processing)
  - Low latency for real time 5G applications
- Scalability and Manageability
  - Orchestration and end-to-end network slicing

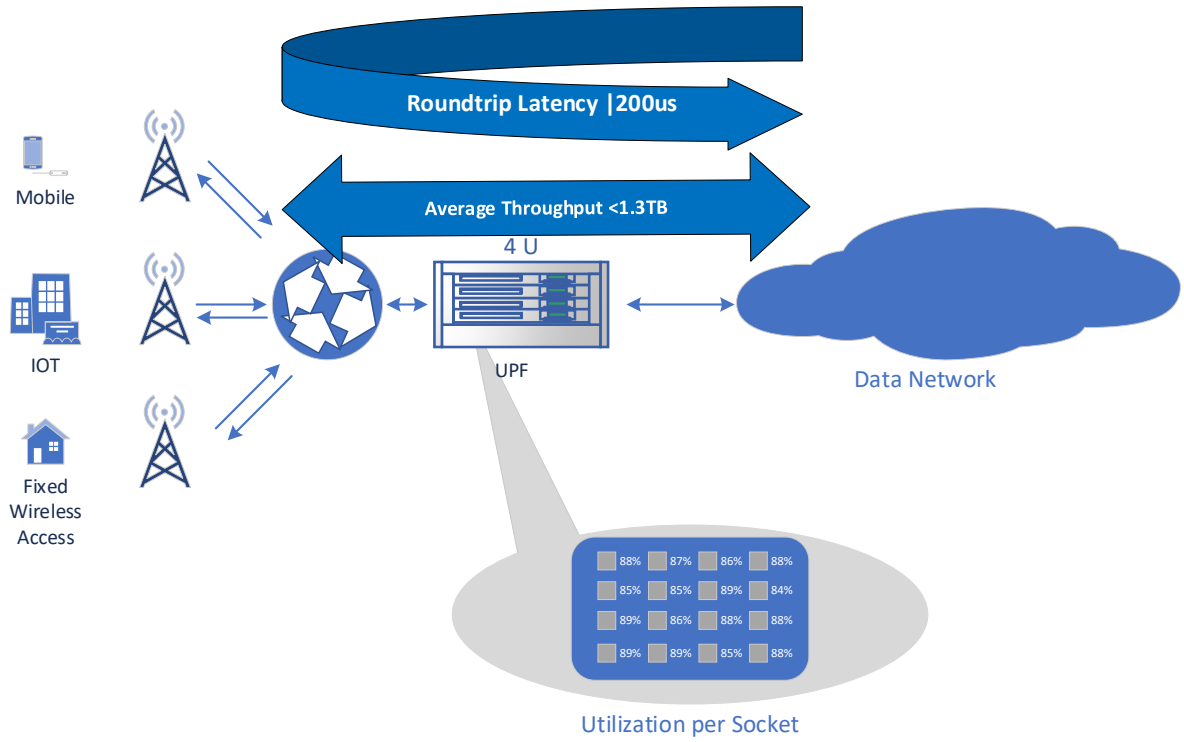
Technologies Implemented

As outlined above, the UPF takes advantage of a number of hardware and software technologies to provide a high and deterministic packet throughput, including the following:

- **Intel® Ethernet Controller 800 Series:** 100G Network Adapter providing a flexible packet processing pipeline to allow for multi-stage parsing, switching and classification of data at the NIC. DDP is a set of workload specific profiles for accelerating pre-processing inline for the Intel® Ethernet Controller 800 Series.
- **2nd generation Intel® Xeon® Scalable processors:** Latest generation Intel® architecture with up to 28 cores to provide high bandwidth throughput, with low latency.
- **DPDK:** Set of data plane libraries and network interface controller poll-mode drivers for accelerating the offload of packet processing from system kernel to processes running in user space. This offloading achieves higher computing efficiency and higher packet throughput by using poll-mode interrupt instead of the interrupt driven processing generally used in kernel space.
- **Kubernetes:** Open-source container-orchestration system for automating application deployment, scaling, and management. It aims to provide a platform for automating deployment, scaling, and operations of application containers across clusters of hosts. It works with a range of container tools, including Docker.
- **collectd*:** Unix* daemon that collects, transfers and stores performance data of platforms and network equipment. The acquired data is meant to help system administrators maintain an overview over available resources to detect existing or looming bottlenecks.
- **Vector Packet Processing (VPP):** VPP is a modular and extensible stack for building high performance network applications, deployed in discrete appliance, virtual machines and the cloud. It is developed using the same type of optimizations as DPDK, allowing for comparably higher performance and greater scalability on Intel® architecture. It implements and accelerates Layer 2, 3, 4 and above protocols, and is used in variety of use cases from IPSEC gateway, load balancer, SDWAN, router, and virtual switch. VPP is robust and well productized in a comprehensive community validation effort called FD.io Continuous System Integration and Testing (CSIT).

Benefits of Solution

We demonstrated a UPF environment with scalability of over 1.3Tbps of network traffic.[1] In addition, the demo also met the key performance indicators required by network operators around latency in a scalable and manageable manner. The performance density significantly improves over previous generations.



As outlined in the diagram above, the UPF is capable of delivering over 1.3Tbps of network traffic in a 4U footprint. In addition, the UPF is capable of providing 5G latency of around 200us. For details on the test configuration, refer to Configuration Details.

Summary

The UPF solution outlined in this paper is highly comparable with existing solutions in the network and provides an efficient, scalable solution on common NFV infrastructure. The 2nd generation Intel® Xeon® Scalable processors and DPDK provide a vectorized packet processing engine to generate a cost effective, powerful user plane, which allows the customers to further scale as network traffic grows.

In addition, the Intel® Ethernet Controller 800 Series provides 100G network interface to allow customers to provide close-to-line-rate into each of the UPF instances, while also allowing users to offload some of the acceleration, classification and scheduling demands from the core.

The solution also provides an overarching management and orchestration framework that allows greater visibility on workload throughput across the network, allowing operators to resolve capacity challenges and enable intelligent scalability of network functions.

REFERENCE	LINK
Hong Kong Applied Science and Technology Research Institute (ASTRI)	www.astri.org
Discover the Difference 5G Core Will Make this Decade Solution Brief	https://builders.intel.com/docs/networkbuilders/discover-the-difference-5g-core-will-make-this-decade.pdf

[1] Refer to Configuration Details for hardware and software details. For more complete information about performance and benchmark results, visit www.intel.com/benchmarks. Refer to http://software.intel.com/en-us/articles/optimization-notice for more information about optimization.

Configuration Details

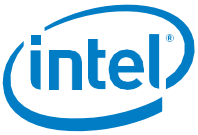
Performance results are based on testing as of 20 December 2019 and may not reflect all publicly available security updates.

Hardware Bill of Materials

ITEM	DESCRIPTION
Platform	Supermicro* BigTwin SYS-2029BT-HNR • 2 x Intel® Xeon® Gold 6230N Processors (24 cores) • 2 x Intel® Ethernet Controller 800 Series 100G NIC (PCIe Gen3.0 x16) • 196GB DDR4 memory
Traffic Generator	Intel® Server Board S2600WF • 2 x Intel® Xeon® Gold 6252N Processor (28 Cores) • 5 x Intel® Ethernet Controller 700 Series 25G NICs • 196GB DDR4 memory

Software Bill of Materials

ITEM	VERSION
Cisco* TRex	v2.41
Kubernetes	v1.13
Container Management for Kubernetes*	v1.3.1
DPDK	19.11
Docker	18.06.1-ce
OS	Ubuntu 18.04
Flannel plugin	V0.9.1
SR-IOV device plugin: https://github.com/intel/sriov-network-device-plugin	V0.1
Multus-CNI plugin	V1.0
Etcd	V3.3.10
Cni-plugins	v0.7.1
Influxdb	V1.3.7
Collectd	V5.10
Vector Packet Processing (VPP) https://fd.io/ **Note:** Astri delivers UPF as a plugin bundled with the VPP release.	V19.07-rc2



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Performance results are based on testing as of dates shown in configurations and may not reflect all publicly available updates. See configuration disclosure for details. No product or component can be absolutely secure.

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