White Paper

Communications Service Providers

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Intel-HPE Verified Reference Configuration for vRAN on the HPE ProLiant DL110 Gen11

intel. Xeon



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Objectives of Intel-HPE VRC for vRAN on HPE ProLiant DL110 Gen11

The telecommunications landscape continues to evolve, driven by the need for improved performance, cost efficiency, flexibility, and more. Open Radio Access Network (Open RAN) technology is one innovative approach gaining momentum and is driven by the decoupling of hardware and software and enabling interoperability, all of which provides operators more flexibility in selection of vendor solutions.

Intel and Hewlett Packard Enterprise (HPE) have been collaborating to enable Open RAN solutions that not only enhance network performance, but also significantly reduce total cost of ownership (TCO). By leveraging the high density, short depth design of the carrier grade HPE ProLiant DL110 Gen11 server that is based on 4th Gen Intel® Xeon® Scalable processors with Intel® vRAN Boost acceleration technology, this collaboration is striving to reshape the telecommunications industry by introducing performance-driven, power-efficient, and highly adaptable Open RAN solutions.

This paper details one of the collaborative initiatives between Intel and HPE to integrate Open RAN technology using the HPE ProLiant DL110 Gen11 server and 4th Gen Intel® Xeon® Scalable processors. The companies have developed a Verified Reference Configuration (VRC) for vRAN which defines the hardware, software and firmware needed to optimize a complete solution for vRAN applications. The reference configuration is based on Intel® FlexRAN[™] reference software that provides full layer 1 processing on Intel® Xeon® Scalable processors. To demonstrate the performance of the reference configuration, this paper describes the configuration and testing of the VRC done by Intel and HPE.

Scope of Intel-HPE VRC for vRAN on the HPE ProLiant DL110 Gen11

Intel has created its verified reference solution program (Figure 1) to provide end users with a comprehensive hardware, firmware, and software foundation for a variety of use cases, including Open RAN. Intel and its partners rigorously test these reference solutions and regularly update them with new customer use cases. The goal is to reduce early integration issues, simplify evaluations, and accelerate time to market.

vRAN Reference Design Test Methodologies

The Intel-HPE Verified Reference Configuration for vRAN used for this paper includes the following items:

- Intel FlexRAN[™] reference software
- Networking
- Virtualization VM using vhost, SR-IOV and SIOV on DPDK-enabled guest
- Containerization
- Data Plane Development Kit (DPDK)

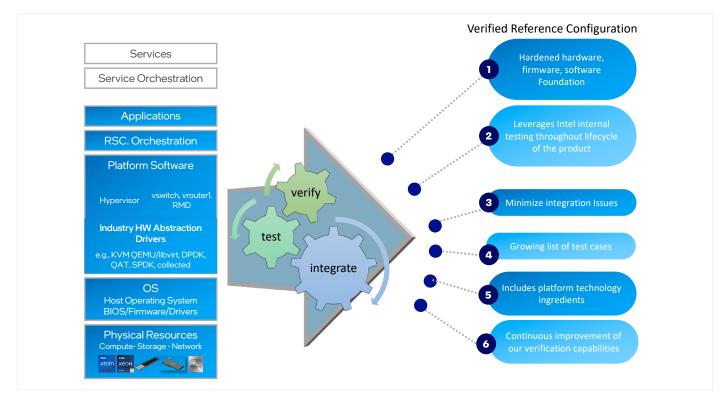


Figure 1. Intel verified reference design process and benefits.

- Intel[®] Data Steaming Accelerator (DSA)
- Platform level testing
- Security and service assurance
- Performance

An Intel VRC is carefully and thoroughly verified by Intel to help ensure the platform configuration in terms of hardware components, BIOS recommendation, and the software solution stack is proven, stable, and reliable for real-time vRAN workloads.

RAN scenarios targeted by VRC for vRAN on the HPE ProLiant DL110 Gen11

The HPE ProLiant DL110 Gen11 platform (Figure 2) is powered by 4th Gen Intel® Xeon® Scalable processors with Intel® vRAN Boost. The server is optimized to run vRAN real-time processing workloads at scale, across distributed and centralized RAN (DRAN, CRAN) deployment scenarios.



Figure 2. Front panel of HPE ProLiant DL110 Gen11 platform.

The Intel-HPE VRC for vRAN targets both midband mMIMO (up to 6x100MHz 64T64R mMIMO) (Figure 3), and narrow band (up to 18x20MHz cell carriers with 4x4 MIMO) (Figure 4) 5G NR deployments.

The same VRC on the HPE ProLiant DL110 Gen11 can underpin many more flavors of RAN sites in terms of RF configurations, fronthaul structure, synchronization, and midhaul architecture.

MIDBAND 6 X 10	LOOMHZ 64T64R RU
E810-CQDA2-2 X 100G	

Figure 3. Midband mMIMO deployment example enabled by Verified Reference Configuration on HPE ProLiant DL110 Gen11.

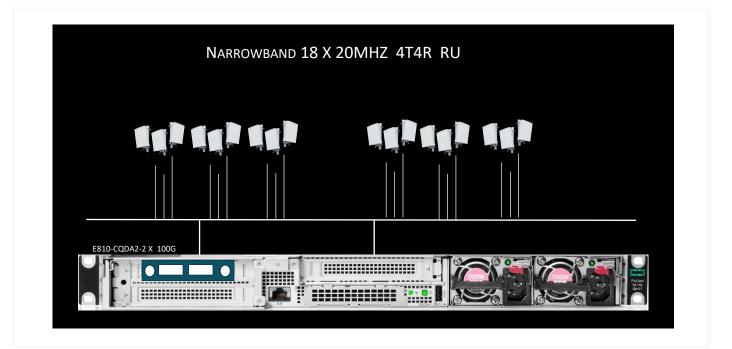


Figure 4. Narrowband deployment example enabled by Verified Reference Configuration.

VRC details for vRAN on HPE ProLiant DL110 Gen11

This section describes the VRC for vRAN on the HPE ProLiant DL110 Gen11, including verified hardware bill of materials and firmware components.

Hardware, firmware of VRC for vRAN on HPE ProLiant DL110 Gen11

The tables below describe the pre-verified hardware and firmware components resulting from Intel-HPE VRC for vRAN on the HPE ProLiant DL110 Gen11.

The hardware bill of materials for VRC for vRAN on the HPE ProLiant DL110 Gen11¹ is described in Table 1.

P54277-B21	HPE DL110 Gen11 Front Cbl CTO Svr	1
BD505A	HPE iLO Adv 1-svr Lic 3yr Support	1
P43150-B21	HPE ProLiant DL110 Gen11 700W FS -48VDC PS Kit] *
P66239-B21	Intel® Xeon® Gold 6433N Processor 32 cores, 2.0 GHz, 205W	1
P43322-B21	HPE 16GB (1x16GB) Single Rank x8 DDR5-4800 R Smart Kit	8
P40513-B21	HPE 480GB NVMe RI M.2 22110 MV SSD	2
P21112-B21	Intel E810-CQDA2 Ethernet 100Gb 2-port QSFP28 Adapter for HPE] **

* - number of PSUs and AC vs DC distribution can be changed to fit concrete deployment scenario

** - number or Ethernet variant of Intel E810 NIC cards can be adjusted to fit concrete fronthaul and synchronization architecture

Configuration of System BIOS and OS within VRC for vRAN on HPE ProLiant DL110 Gen11

Proper configuration of system BIOS, kernel and operating system are important to achieve deterministic low latency system behavior essential for real time vRAN baseband processing workloads, all while keeping power consumption as low as possible.

As a guiding strategy in optimizing the Unified Extensible Firmware Interface (UEFI) profile for required behavior under real time baseband processing vRAN workload, the Intel-HPE VRC program leveraged general recommendations for BIOS setting for FlexRAN[™] reference architecture for 4th Gen Intel[®] Xeon[®] Scalable processors with Intel[®] vRAN Boost. This BIOS tuning strategy has been translated to proper server workload profile for HPE ProLiant DL110 Gen11.

Intel BIOS recommendation for FlexRAN[™] reference architecture platform

Intel recommends using the BIOS settings for max performance with low latency configuration to meet the optimized deterministic performance requirements for the vRAN reference implementation.

Refer to document BIOS Settings for FlexRAN[™] reference architecture platforms based on Intel[®] Xeon[®] Scalable processors (#640685) for information on the BIOS settings.

HPE ProLiant DL110 Gen11 BIOS Configuration

The HPE ProLiant DL110 provides predefined VRAN workload profiles (Figure 5), aligned with 4th Gen Intel® Xeon® Scalable processor recommendation for optimal performance of VRAN workloads. FlexRAN Reference L1 Implementation has leveraged the vRAN workload profile for the VRC program.

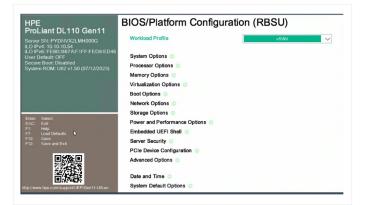


Figure 5. vRAN BIOS configuration recommendations.

VRC for vRAN on the HPE ProLiant DL110 Gen11 Testing Setup

Before testing the actual vRAN workload, a foundational set of tests was executed as part of the VRC for vRAN on HPE ProLiant DL110 Gen11 to establish a solid baseline.

Foundational tests

The following foundational tests are recommended and have been executed as part of the VRC for vRAN on HPE ProLiant DL110 Gen11:

MLC

The first application is the memory latency checker, which can be downloaded from https://software.intel.com/en-us/articles/intelr-memory-latency-checker.

Download the latest version and execute this application, unzip the tarball package and go into Linux folder and execute ./mlc

Jitter

The jitter application aims to measure the variability of latency in the execution of a user space dummy loop with dummy operation, more information about this tool is available at https://wiki.fd.io/view/Pma_tools/jitter

Use the following steps to download the tool, build, and execute the tool targeting an idle core:

- git clone https://gerrit.fd.io/r/pma_tools
- cd pma_tools/jitter
- make
- ./jitter –c 2 –i 200

Review Inst_Jitter column, using deterministic performance in a BIOS setting, the jitter should not exceed 10,000.

• Cyclictest vRAN DU/CU solutions require vRAN system latency and responsiveness to be very low (e.g., below approximate to 10us over 12-24 hours period). The Cyclictest application is used to measure this latency.

Following setup of Cyclictest is recommended:

After 24hrs test, the max latency should be under 10us as shown below:

test	duration (hour)	min	avg	max
cyclictest	12	2	2	5
cyclictest	24	2	2	5

Tests were conducted by Intel in Aug. 2023 and involved testing on a bare metal with Ubuntu RT kernel command line: BOOT_IMAGE=/boot/vmlinuz-5.15.0-1032-realtime root=UUID=15d349a6-f87a-4d14-83a7-1518eadbf21b ro default_hugepagesz=1G hugepages=30 hugepagesz=1G intel_iommu=on iommu=pt skew_tick=1 isolcpus=managed_irq,domain,1-30,33-62 nohz_full=1-30,33-62 nohz=on rcu_nocbs=1-30,33-62 rcu_nocb_poll nosoftlockup nmi_watchdog=0 crashkernel=auto selinux=0 mce=off audit=0 vfio_pci.enable_sriov=1 vfio_pci.disable_idle_d3=1 usbcore. autosuspend=-1 tsc=reliable intel_idle.max_cstate=0

The above set of foundational tests ensures low latency deterministic behavior of the HPE ProLiant DL110 Gen11 system and provides a foundation upon further verification of vRAN workload rests.

PHY Acceleration tests

A production-grade, high-capacity vRAN solution benefits from offloading the forward error control (FEC) of higher PHY baseband processing to a dedicated accelerator.

The recommended architectural approach within Intel-HPE VRC for vRAN on the HPE ProLiant DL110 Gen11 is to offload 5G NR LDPC and/or 4G LTE Turbo coding/decoding functionality into the 4th Gen Intel® Xeon® Scalable Processor with Intel® vRAN Boost technology as a dedicated accelerator.

From a software acceleration standpoint, the system leverages DPDK BBDEV extension as an open API between vDU application.

Verifying the functional capabilities and the performance of Intel[®] vRAN Boost FEC accelerator together with DPDK BBDEV API is an important step in the Intel VRC for vRAN on the HPE ProLiant DL110 Gen11:

BBDEV-test

The dpdk-test-bbdev tool is a DPDK utility that allows measuring functional capability parameters of PMDs available in the BBDEV framework. Tests for execution are latency, throughput, validation, block error rate (Block error rate, ratio of blocks not decoded at a given signal to noise ratio (SNR)), and sanity tests. Execution of tests can be customized using various parameters passed to a python running script.

There are 6 main test cases to be executed using bbdev-test tool:

- 1. Validation tests [-c validation]
- Performs full operation of enqueue and dequeue
- Compares the dequeued data buffer with expected values in the test vector (TV) being used
- Fails if any dequeued value does not match the data in the TV
- 2. Offload cost measurement [-c offload]
- Measures the CPU cycles consumed from the receipt of a user enqueue until it is put on the device queue

- 3. Latency measurement [-c latency]
- Measures the time consumed from the first enqueue until the first appearance of a dequeued result
- This measurement represents the full latency of a bbdev operation (encode or decode) to execute
- 4. Poll-mode throughput measurement [-c throughput]
- Performs full operation of enqueue and dequeue
- Executes in poll mode
- Measures the achieved throughput on a subset of available cores or all available CPU cores
- Dequeued data is not validated against expected values stored in TV

- Results are printed in million operations per second and million bits per second
- 5. BLER measurement [-c bler]
- Performs full operation of enqueue and dequeue
- Measures the achieved throughput on a subset or all available CPU cores
- Computed BLER as a percentage based on the total number of operations
- 6. Interrupt-mode throughput [-c interrupt]
- Similar to throughput test case but using interrupts. No polling.

Scripts:

```
python3 ./test-bbdev.py -e="-c 0xff0 -a${PCI_ADDR} --vfio-vf-token=${VF_TOKEN}" -n 60 -b 24 -l 4 -t 10 -c validation -v ./test_vectors/* >> test_report
python3 ./test-bbdev.py -e="-c 0xff0 -a${PCI_ADDR} --vfio-vf-token=${VF_TOKEN}" -n 80 -b 64 -l 1 -t 10 -c latency -v ./test_vectors/* >> test_report
python3 ./test-bbdev.py -e="-c 0xff0 -a${PCI_ADDR} --vfio-vf-token=${VF_TOKEN}" -n 100 -b 80 -l 1 -t 10 -c throughput -v ./test_vectors/* >> test_report
python3 ./test-bbdev.py -e="-c 0xff0 -a${PCI_ADDR} --vfio-vf-token=${VF_TOKEN}" -n 50 -b 32 -l 1 -t 10 -c offload -v ./test_vectors/* >> test_report
python3 ./test-bbdev.py -e="-c 0xff0 -a${PCI_ADDR} --vfio-vf-token=${VF_TOKEN}" -n 70 -b 50 -l 1 -t 10 -c offload -v ./test_vectors/* >> test_report
python3 ./test-bbdev.py -e="-c 0xff0 -a${PCI_ADDR} --vfio-vf-token=${VF_TOKEN}" -n 70 -b 50 -l 1 -t 10 -c offload -v ./test_vectors/* >> test_report
python3 ./test-bbdev.py -e="-c 0xff0 -a${PCI_ADDR} --vfio-vf-token=${VF_TOKEN}" -n 70 -b 50 -l 1 -t 10 -c interrupt -v ./test_vectors/* >> test_report
python3 ./test-bbdev.py -e="-c 0xff0 -a${PCI_ADDR} --vfio-vf-token=${VF_TOKEN}" -n 10 -b 10 -l 1 -t 10 -c interrupt -v ./test_vectors/1 >> test_report
```

Ensure that the result from the print log does not show any failing results in each test. Some tests are skipped because they are not supported by the device - this does not impact vRAN functionality or performance.

DPDK-test-bbdev app

DPDK-test-bbdev-app is a test tool to enable execution of only the uplink (UL) and downlink (DL) Low Density Parity Check Code (LDPC) operations in a loop for any given cell configuration on the LDPC hardware (without the rest of the L1 pipeline). This can be used notably for measuring hardware performance and power operations management. It is included in the FlexRAN[™] reference software release.

vRAN workload tests with Intel FlexRAN[™] reference architecture

Intel's FlexRAN[™] reference architecture is a flexible and scalable open RAN reference implementation for Intel® Xeon® Scalable based servers. The FlexRAN reference architecture refers to both the reference instance, as well as the baseband software and supports both bare metal as well as virtualized and cloud RAN topologies. FlexRAN[™] reference software optimizes the use of Intel® Xeon® Scalable processors and accelerators to fully realize a high-performance vRAN base station on a general-purpose compute platform.

The FlexRAN[™] reference architecture has been widely adopted by a diverse ecosystem of RAN players and has been used within the Intel-HPE VRC for vRAN on the HPE ProLiant DL110 Gen11 as the vRAN workload representation for functional and performance tests. Within the testing setup, verification of consistent performance for representative (instead of concrete) RAN configurations (e.g., 6x100MHz mMIMO 64x64) were executed on HPE ProLiant DL110 Gen11 using Testmac in timer mode operation. Testmac is a standalone testing tool without any external dependency to third-party software or hardware components. The L1 application is run in real-time mode and source of time (for TTI / symbol boundaries) is based on the Intel® Xeon® Scalable processor's internal timestamp counter.

The samples are read from reference files (from test config) and loaded into system memory (DDR). The L1 application reads from, and writes to, memory. The cycle count is used as a form of performance, where time stamps are logged through every event in the pipeline and stored.

In this mode:

- There are no external dependencies in terms of hardware or third-party software components.
- The L1 application is run in real-time mode and source of time (for TTI / symbol boundaries) is the Intel[®] Xeon[®] Scalable processor's internal time stamp counter.
- The IQ samples are read from reference files (from test config) and loaded into DDR and L1 application reads from and writes to memory.
- This mode is used for cycle count performance benchmarking where time stamps are logged through every event in the pipeline and stored.

VRC for vRAN on HPE ProLiant DL110 Gen11, Testing Results Overview

Some of the key foundational testing results and functional tests for the pre-integrated VRC for vRAN on HPE ProLiant DL110 Gen11 are provided in figures 6 and 7:

BBDEV test

100% pass rate for the key 6 metrics of acceleration:

python3 ./test-bbdev.py -e="-c 0xff0 -a70:00.0" -n 60 -b 24 -l 4 -c validation -v ./ <u>test_vectors</u> /* >> <u>test_report</u>	
[root@localhost test-bbdev]# cat test_report grep -v Debug grep Passed awk '{sum += \$5} END {print "P:" sum}' P:33	
root@localhost test-bbdev]# cat test_report grep -v Debug grep Failed awk '{sum += \$5} END {print "F:" sum}' F:θ	Result:
oython3 ./test-bbdev.py -e="-c 0xff0 -a70:00.0" -n 80 -b 64 -l 1 -t 10 -c latency -v ./test .vectors/* >> test .report	Validation: Pass 33, Fail 0
<pre>[root@localhost test-bbdev]# cat test_report grep -v Debug grep Passed awk '{sum += \$5} END {print "P:" sum}' P:33 [root@localhost test bbdev]# cat test_report grep -v Debug grep Passed awk '{sum += \$5} END {print "P:" sum}'</pre>	
<pre>[root@localhost test-bbdev]# cat test_report grep -v Debug grep Failed awk '{sum += \$5} END {print "F:" sum}' F:0</pre>	
oython3 ./test-bbdev.py -e=" c 0xff0 -a70:00.0" -n 100 -b 80 -l 1 -t 10 -c throughput -v ./test_vectors/* >> test_report	Latency: Pass 33 Fail 0
[root@localhost test-bbdev]# cat test_report grep -v Debug grep Passed awk '{sum += \$5} END {print "P:" sum}' P:33 [root@localhost test-bbdev]# cat test_report grep -v Debug grep Failed awk '{sum += \$5} END {print "F:" sum}'	
F10 bython3 ./test-bbdev.py -e="-c 0xff0 -a70:00.0" -n 50 -b 32 -l 1 -c offload -v ./ <u>test_vectors/* >> test_report</u>	Throughput: Pass 33 Fail 0
(root@localhost test-bbdev)# cat test_report grep •v Debug grep Passed awk '{sum += \$5} END {print "P:" sum}' P:66	
root@localhost test-bbdev]# cat test_report grep -v Debug grep Failed awk '{sum += \$5} END {print "F:" sum}' F:0	Offload: Pass 66 Fail 0
oython3 ./test-bbdev.py -e="-c 0xff0 -a70:00.0" -n 70 -b 50 -l 1 -c bler -v ./test_vectors/l* >> test_report	Ontoau. Pass 00 Fait 0
[root@localhost test-bbdev]# cat test_report grep -v Debug grep Passed awk '{sum += \$5} END {print "P:" sum}' P:17	
<pre>[root@localhost test-bbdev]# cat test_report grep -v Debug grep Failed awk '{sum += \$5} END {print "F:" sum}' F:0</pre>	BLER: Pass 17 Fail 0
python3 ./test-bbdev.py -e="-c 0xff -a70:00.0" -n 10 -b 10 -l 1 -c interrupt -v ./ <u>test_vectors</u> /l* >> <u>test_report</u>	
[root@localhost test-bbdev]# cat test_report grep -v Debug grep Passed awk '{sum += \$5} END {print "P:" sum}' P:	Interrupt: Pass 0 Fail 0
[root@localhost test-bbdev]# cat test_report grep -v Debug grep Failed awk '{sum += \$5} END {print "F:" sum}' e-	interrupt. Fass O Fait O

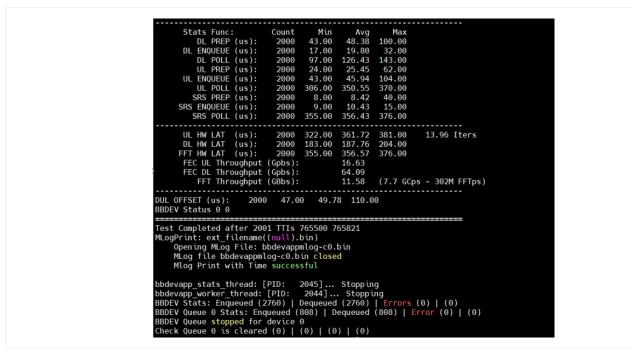
Figure 6. BBDEV test results showing pass rate of verified reference configuration platform.

est Result:	
'assed:225	
ailed:0	
kipped:190	
oot@npx:/home/flexran/flexran/dpdk-stable-22.11.1/app/test-bbdev#	

Figure 7. BBDEV test results showing pass rate of verified reference configuration platform.

BBDEV app

Figure 8 shows stable results of BBDEV application, with no exceptions in the output logs.



Intel[®] FlexRAN[™] Reference Software Massive MIMO testing

The HPE ProLiant DL110 Gen11 has been verified for midband mMIMO configuration, 6x100MHz 64x64. Results can be provided upon request.

CONFIGURATION	USE CASE: MMIMO 100MHZ 64T64R
Test Config / Test Case	HPE ProLiant DL110 Gen11 system with Intel® Xeon® Gold 6433N Processor
LDPC Offload	Intel® vRAN Boost
Number of Cells	6

Platform integration functional verification

As a foundational effort, Intel used integration functional testing to verify the HPE ProLiant DL110 Gen11 compute platform, it's hardware and firmware components, drivers, and the Intel[®] FlexRAN[™] reference software. The table below summarizes the 100% pass rate of functional tests for the VRC recipe of components:

	TESTS ATTEMPTED	TESTS PASSED	TESTS FAILED	PASS RATE,%
DPDK_Columbiaville_100G	89	89	0	100%
Intel® Data Streaming Accelerator (DSA)	24	24	0	100%
Intel [®] FlexRAN [™] reference software	22	22	0	100%
Platform	4	4	0	100%
Intel® Software Guard Executions (SGX)	10	10	0	100%
Intel® Speed Select - Core Power (Intel® SST-CP)	4	4	0	100%
Single Root of IO Virtualization (SR-IOV)	11	11	0	100%
Virtualization (virtio_vhost)	6	6	0	100%

Conclusion

HPE and Intel have delivered a high performing VRC for the vRAN workload using the HPE ProLiant DL110 Gen11 platform based on the 4th Gen Intel® Xeon® Scalable processors with Intel® vRAN Boost. Through this close collaboration, the companies have detailed in this paper the multiple system tests used to validate the performance of the VRC vRAN configurations with open components and a VRC which is tuned for optimal performance.

As the telecommunications landscape continues to evolve driven by telecom operator and end user requirements, Intel and HPE will continue their close collaboration. The joint objectives of the tight collaboration continues to be to reduce the risk of deploying open solutions on general purpose servers like the HPE ProLiant DL110, reduce the complexity through Intel innovation, and achieve the goal of providing optimal performance, flexibility, and a better TCO for our customers. White Paper | Intel-HPE Verified Reference Configuration for vRAN on the HPE ProLiant DL110 Gen11



 1 HPE ProLiant DL110 Gen11 firmware and software solution stacks for VRC details can be provided upon request through your field representative.

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