White Paper

Communications Service Providers
Deep Packet Inspection

Rohde & Schwarz Tests Deep Packet Inspection for 5G Networks

Tests of R&S®PACE 2 DPI performance show 33.8%[1] increase on Intel® Xeon® Scalable processor-based servers and the performance impact between aligned vs. misaligned non-uniform memory access (NUMA) in dual socket systems

ROHDE&SCHWARZ
Make ideas real

Deep packet inspection (DPI) is a critical element of 4G/5G wireless networks as it is mandatory for application awareness and flow prioritization for proper service delivery and high quality of experience. Typically a mobile network operator (MNO) will run all data flows through a DPI engine, which makes the performance of the DPI engine important because it can't introduce latency or reduce throughput.

Many MNOs built out their DPI infrastructures on 4G networks and now need to know if upgrading servers is required to keep up with the faster data speeds of 5G networks. Working with Intel® Network Builders, ipoque, a Rohde & Schwarz company, has devised two performance tests. The first test demonstrates how performance improves when upgrading to Intel® Xeon® Scalable processors. Overall, the tests showed a 33.8% performance increase when upgrading to a new CPU.[1]

The second test demonstrated the performance reduction when non-uniform memory alignment (NUMA), is not properly configured. Dual-socket servers deliver added DPI performance needed to meet the higher packet throughput of 5G networks. NUMA configuration is imperative to achieve maximum performance for multi-socket servers. Rohde & Schwarz also tested the performance impact of a misaligned NUMA worker thread to highlight the impact this error can have on overall system performance. The tests found that having such a misalignment can denigrate DPI throughput performance by 25.4%.[1]

DPI Enables Application Awareness, Network Analytics

DPI became an integral part of MNO traffic management systems for their 4G networks and is even more important for 5G networks. 5G offers a big increase in mobile data throughput—with theoretical throughput up to 50 Gbps[2]—and a significant reduction in latency that will drive new applications for mobile devices, Internet of Things (IoT) sensors, and for fixed broadband wireless services. In conjunction with the network improvements, other technologies such as machine learning and edge cloud computing open up brand new services when combined with a high-speed 5G wireless data link.

4G networks have complicated data flows for DPI analysis, a challenge that is expected to be the same for 5G networks. The average smartphone has more than 50 applications on it, many transmitting with encrypted secure sockets layer (SSL) or Quick UDP Internet Connections (QUIC) protocols. Processing these data flows requires a sophisticated DPI solution that features performance for ever-changing packet flows.

DPI can examine and extract data from layers 3-7 and beyond of the OSI-layer stack on a per-packet basis to provide application awareness (see Figure 1). MNOs can better understand the different types of traffic in their networks, allowing for effective application monitoring and dynamic traffic management for enhanced network performance.

Table of Contents

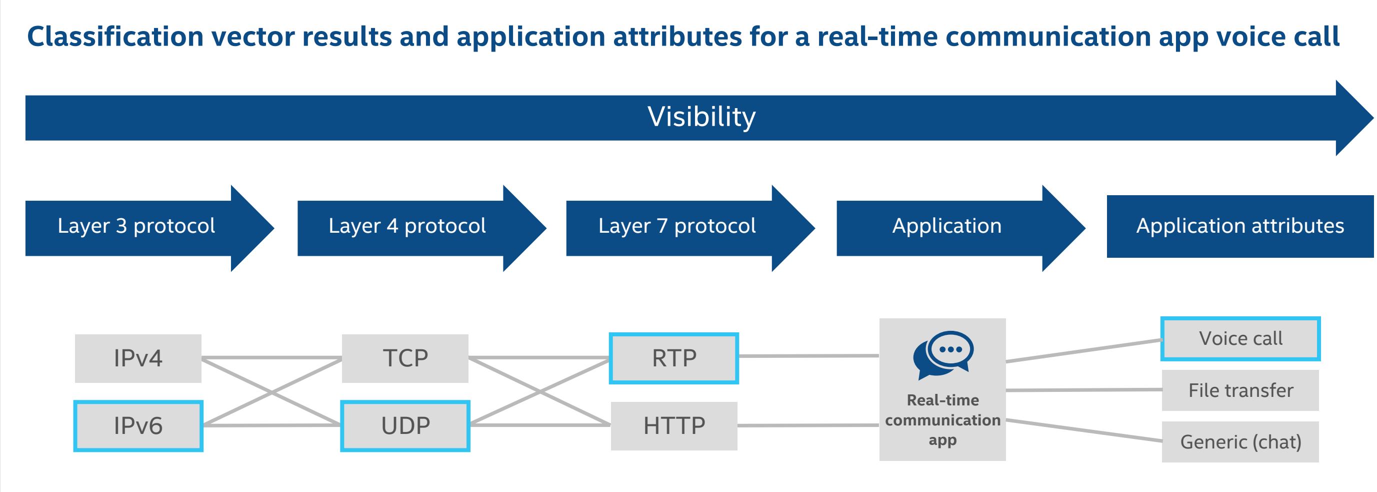

Figure 1. R&S®PACE 2 DPI solution looks deep into packets to uncover applications and application attributes needed for application awareness.

In addition to application awareness, DPI provides real-time traffic classification information feeds to network traffic analytics programs on a per-service basis for new 5G services like network slicing, and applications such as edge networking use cases. 5G networks need the information from DPI engines in order to respond to network conditions that could impact quality of service or quality of experience.

R&S®PACE 2 OEM DPI Software Solution

R&S®PACE 2 is a DPI and IP traffic analytics engine that brings application awareness capabilities to network analytics, traffic management, and network security solutions. DPI is only one of the libraries of software solutions offered by R&S®PACE 2, which also include behavioral, heuristic, and statistical analysis. Combined, these functions reliably detect network protocols and applications and extract metadata in real time.

The R&S®PACE 2 architecture processes packets and extracts metadata in five stages using a polling API. The stages (see Figure 2) include the following:

Packet preparation: This initial stage builds up the frame stack, decapsulizes the protocol, and provides IP defragmentation in order to send out a packet that can be processed by the following stages.

Packet reordering: The packet reordering engine is an optional stage that buffers and reorders packets that have arrived out of order. Once the missing packets arrive, the data stream will be forwarded with packets in appropriate order. This step has an impact on the detection classification rate.

Packet classification: The packet classification stage provides the protocol and application detection results, as well as network performance metadata. The packet classification includes a high number of different protocol and application detections.

Packet decoding: Packet decoding provides advanced metadata as well as content decoding on a per-packet basis. If this stage is used, it is possible to extract detailed metadata in real time.

Timeout handling: This stage primarily provides timeout events from the decoder and should be called even if the current packet was buffered in the packet reordering stage. If internal flow or subscriber tracking is used, these timeout events will be returned by this stage as well.

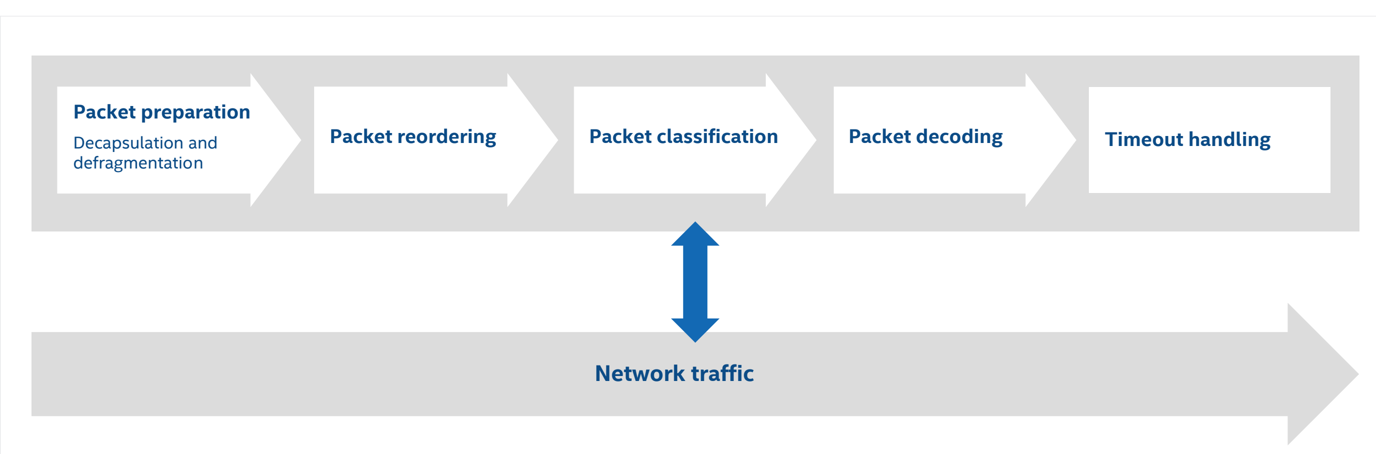

Figure 2. Five processing stages of R&S®PACE 2 architecture.

The software is integrated into network analytics, traffic management, and network security solutions, and classifies thousands of applications and protocols. R&S®PACE 2 provides content and metadata extraction and delivers crucial information from IP traffic based on metrics and heuristics.

Key applications for the software include the following:

- Virtual enhanced packet core (vEPC)
- Software defined WAN
- Video streaming optimization
- Wireless access points
- Network security (IDS/IPS, next generation firewalls, SIEM, UTM)
- Network monitoring and traffic management
- Policy and charging
- Application delivery and optimization
- Analytics
- Mobile data offload

The DPI engine can classify IP traffic even if advanced obfuscation and encryption techniques are used. R&S®PACE 2 is a critical enabler for a more secure, reliable, and efficient network.

Test Results

Rohde & Schwarz conducted two tests to highlight performance of the R&S®PACE 2:

- A head-to-head performance comparison between servers based on Intel Xeon E5 processors and Intel Xeon Scalable processors. The goal was to show just how much the performance increased so MNOs could see how this upgrade could impact their networks.
- A live traffic scenario test—using one server as traffic generator and a second server as a device under test (DUT)—of a NUMA-configured system that illustrates the performance cost of a NUMA misalignment.

Test 1: Performance Comparison

The first test compared the performance on DUT Configuration A, a server powered by two Intel Xeon E5-2699 v4 CPUs, with DUT Configuration B, a server powered by two Intel Xeon Scalable Gold 6230N processors.

The test case consisted of live traffic profiles recorded in form of pcap samples that were stored into a ramdisk of the DUT. The actual network traffic profiles are representative of three different customer traffic types:

- Mobile network operator traffic from an enhanced packet core (EPC)
- Enterprise office applications transmitted, including several virtual private network (VPN) tunnels
- Streaming live television, music, and video services
- A mixed DPI data profile comprising a variety of common applications (social media, video streaming, music streaming, and others) that is compatible with TRex traffic generator (as used in test case 2)

Some of the other test setup parameters included the following:

- Flow and subscriber tracking within time-ordered hash tables
- DPI full classification enabled
- Handing over remaining packets of a flow into external fastpath upon classification
- Support of thousands of classification signatures based on different applications, protocols, and attributes
- R&S Application runs on one physical/logical core in order to gather median throughput per logical core
- The test cases were repeated 20 times and results statistically postprocessed using the statistical capabilities of the GNU datamash tool.

The results of this test can be seen in Figure 3:

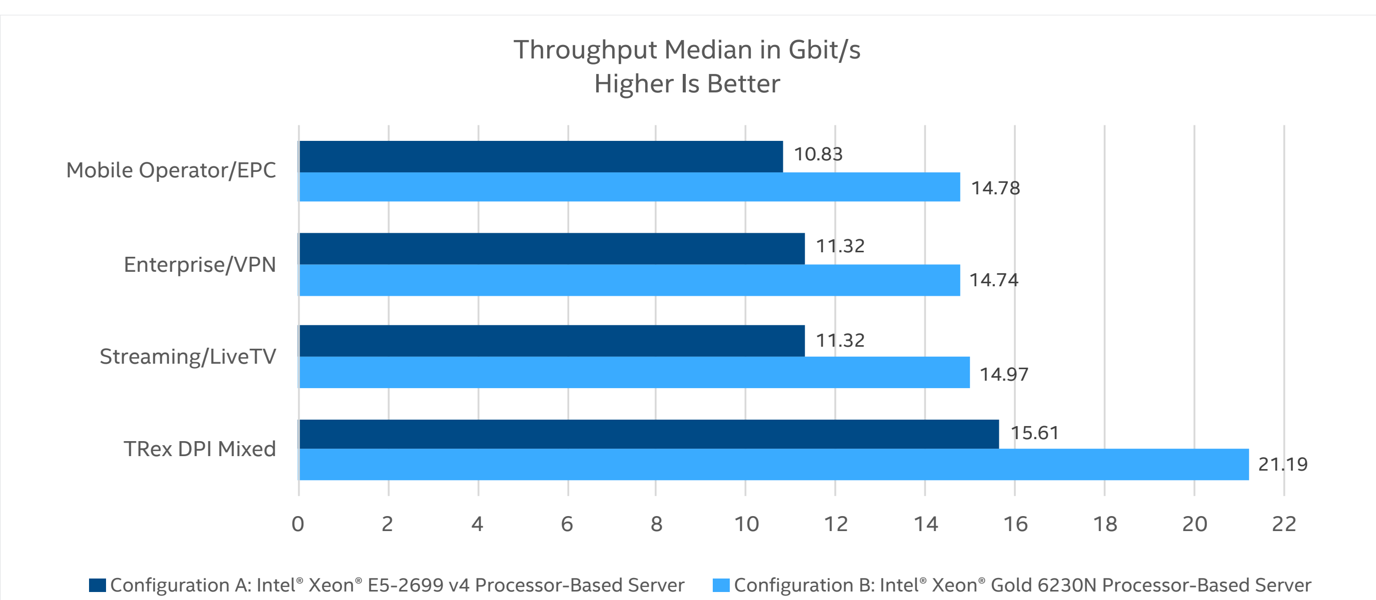

Figure 3. Configuration A and Configuration B throughput per network traffic profile. Measured on 1 logical core.

The results of the test show that newer Intel Xeon Scalable Gold 6230N processors drive a 33.8% increase in DPI performance (as measured by the calculated mean speedup across the four workload) over the server powered by the Intel Xeon E5-2699 v4 processor. For companies that evaluate DPI upgrades on a cost-per-transmitted-bit analysis, the performance increase will drive a significant value. And for some high throughput data flows, like 5G, the performance alone will be necessary.

Test 2: NUMA Misalignment

A dual-socket server brings added performance to a DPI processing, and the proper configuration of DPI thread instances towards the NUMA-aligned memory banks is imperative. Misalignments can be costly in terms of performance. The second test looked at the impact of a NUMA misalignment in terms of reduced performance.

NUMA is a shared memory architecture that describes the placement of main memory modules with respect to processors in a multiprocessor system. Like most every other processor architectural feature, ignorance of NUMA can result in sub-par application memory performance.

R&S®PACE 2 supports an integration using NUMA-aware sub-initialization functions for each worker thread. This is recommended on NUMA architectures to allocate requested memory that is directly associated with the node of the thread.

Not making these allocations can result in all necessary processing data, such as tracking tables, being misplaced on the wrong memory location. In this case, the remaining processing threads are distributed over all nodes of a system, and the necessary data for processing has to be transferred over the Intel® QuickPath Interconnect (Intel® QPI) bus to be available on the processing CPU. This results in a higher workload of the bus and lower overall performance of the system.

The DUT with the Configuration B server utilized Intel Xeon Scalable 6230N CPUs. It was configured with both the R&S®PACE 2 DPI function and l2fwd, a packet forwarding test application that is part of the Data Plane Development Kit (DPDK). As seen in Figure 4, the TRex traffic generator generated stateful and bidirectional traffic on NIC 18:00.0 and 18:00.1, which is received and replied to on the DUT NICs 88:00.0 and 88:00:1. Hence the traffic generator application is capable of gathering performance metrics like traffic throughput, latency, and potential packet loss upon exceeding throughput limits.

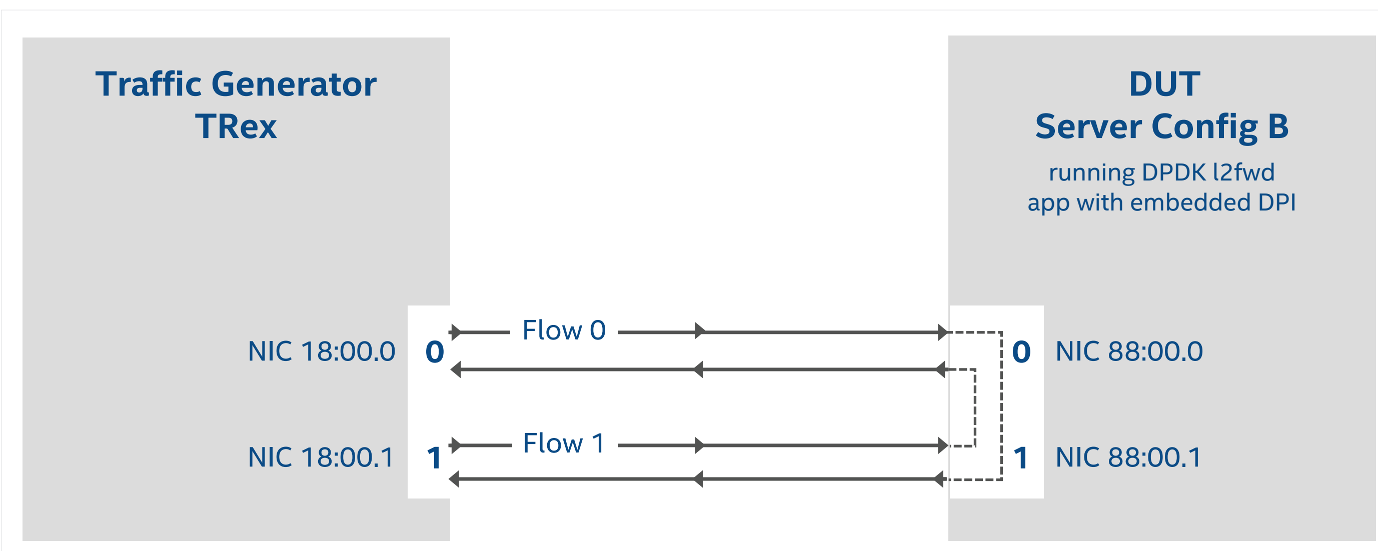

Figure 4. Setup for Test 2.

Key Benefits of R&S®PACE 2

- Reduced time to market and save costs: software is ready for integration, reducing development time and capital and operational expenditures
- Easy and fast integration: highly flexible and platform-agnostic API for integration with no external dependencies
- Highly efficient memory consumption
- Coverage: support for thousands of protocols and applications across diverse operating systems, application versions, and service types
- Metadata extraction: deeper insight on application attributes, for example, quality of service/quality of experience key performance indicators on network performance and applications such as voice over internet protocol (VoIP) and video
- Frequent signature updates, including new additions to classification library
- Deployed globally as OEM in global mobile networks, which provides better visibility and detection rate of applications

Tests were then run using pre-configured YAML files from TRex both with a NUMA misalignment configured in the DUT and without. The first three data flows (rtsp_full2.yaml, sfr3.yaml, and lb_exl.yaml) in each graph in Figure 5 are not DPI relevant and only feature slight performance differences. They were used to illustrate the misalignment impact on a variety of traffic profiles.

The last data flow on Figure 5 (mixed_dpi.yaml) shows a special DPI traffic flow and that is where the misalignment has the biggest impact. For the non-DPI data flows, like rtsp or sfr3.yaml, there is significantly less memory access into the DPI hash tables required, which results in lower loads on the Intel QPI. The graphs in Figure 5 show the impact of the misalignment both in Gbps and in millions of packets per second (Mpps):

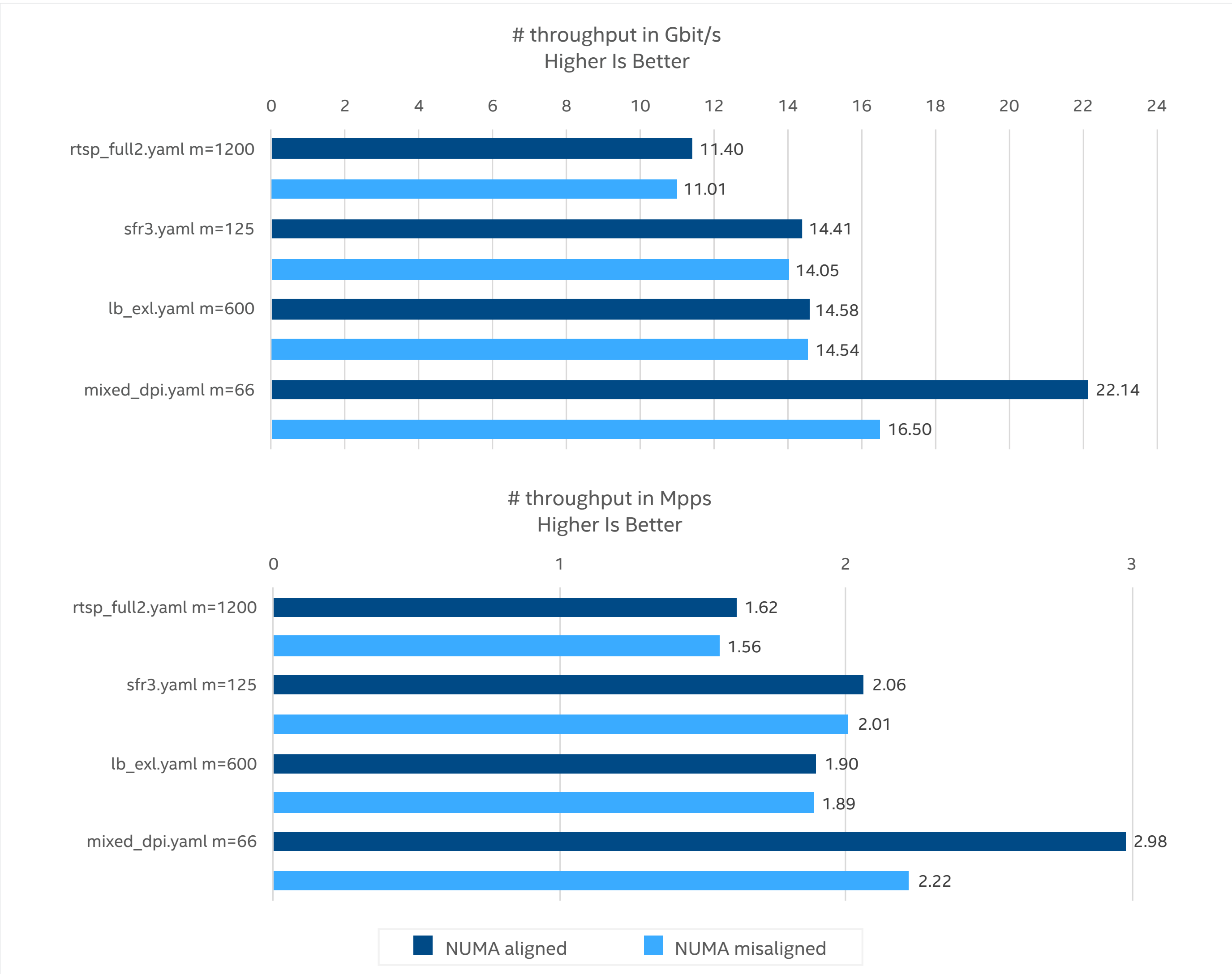

Figure 5. Test 2 results measured in Gbps and Mpps. Measured on 1 logical core.

Tests were then run using pre-configured YAML files from TRex both with a NUMA misalignment configured in the DUT and without. The first three data flows (rtsp_full2.yaml, sfr3.yaml, and lb_exl.yaml) in each graph in Figure 6 are not DPI relevant and only feature slight performance differences. They were used to illustrate the misalignment impact on a variety of traffic profiles.

The last data flow on Figure 6 (mixed_dpi.yaml) shows a special DPI traffic flow and that is where the misalignment has the biggest impact. For the non-DPI data flows, like rtsp or sfr3.yaml, there is significantly less memory access into the DPI hash tables required, which results in lower loads on the Intel QPI. The graphs in Figure 6 show the impact of the misalignment both in Gbps and in millions of packets per second (Mpps):

Overall, the impact of the test is that a misaligned NUMA worker thread can cause up to a 25.4% drop in throughput on a server powered by an Intel Xeon Scalable Gold 6230N CPU.

Conclusion

DPI is an essential element of 5G network deployments and with R&S®PACE 2, MNOs have the ability to enable dynamic traffic management policies that are responsive to each traffic type. More specifically, R&S®PACE 2 DPI enables deployments of advanced 5G services such as:

- 5G service classes (emBB, URLLC, mMTC)
- 5G network slicing
- 5G vRAN
- 5G network virtualization and programmability
- 5G network edge

The R&S®PACE 2 DPI engine can be embedded in software to enable real-time network visibility, application awareness, and network analytics. Tests done by Rohde & Schwarz show that moving from a 4G-era server to the latest Intel Xeon Scalable server can provide significant performance benefits for 5G network deployments. In addition, by properly configuring the NUMA implementation, MNOs can avoid performance declines that are common with misalignments.

These tests show that a properly optimized R&S®PACE 2 implementation, running on Intel® architecture-based servers, can help optimize the real time DPI performance to accommodate the higher data throughput of 5G networks.

More Information

R&S®PACE 2 from ipoque, a Rohde & Schwarz company: https://www.ipoque.com/products/dpi-engine-rs-pace2

Rohde & Schwarz is a member of the Intel® Network Builders ecosystem:
https://networkbuilders.intel.com/ecosystem/rohde-and-schwarz

Intel® Xeon® Scalable processors: http://intel.com/xeon

Notices & Disclaimers

[1] Tested by Rohde & Schwarz in May 2020. Device under test Configuration A hardware was an Intel server board (Intel® Server Board S2600WTT) powered by two Intel® Xeon® E5-2699 v4 CPUs (0xb000038), with 256 GB of memory (16 GB 2133 MHz PC4-17000 DDR4 memory modules), one 240 GB Intel® Solid State Drive Data Center S3520 Series SATA and one 4 TB SATA hard drive. Networking was provided by one onboard Intel® Ethernet Network Controller X540 with dual 10 GbE ports. Software: The DUT ran the R&S®PACE 2 (x86_64bit__version_20.01.24) for DPI with CentOS Linux release 7.8-2003 as the operating system (kernel: 3.10.0-957.el7.x86_64). Compiler gcc version 4.8.5, and libraries include GLIBC 2.17.

DUT Configuration B hardware was an Intel server board (Intel® Server System R2208WFQZS) powered by two Intel Xeon Scalable Gold 6230N processors (0x500002c), with 384GB of memory (24 16 GB 2666 DDR4 memory modules), 2 512 GB SSD M.2 SATA 3.0 drives along with four Intel SSD DC P4510 Series 1.0TB SSD PCIe NVMe 3.0 drives. Networking was provided by four Intel® Ethernet Network Adapter XXV710-DA2 dual port 25 GbE Ethernet controllers. Software: The DUT ran the R&S®PACE 2 for DPI (x86_64bit__version_20.01.24) with Ubuntu 18.04.2 LTS Server as the operating system (kernel: 4.15.0-48-generic #51-Ubuntu). DPDK version was DPDK 19.11.1 LTS, compiler gcc version 7.3.0, and libraries include GLIBC 2.27.

[2] https://5g.co.uk/guides/how-fast-is-5g/

0920/DO/H09/PDF Please Recycle 344585-001US