Silicom FEC Acceleration Adapter Designed for 4G & 5G Networks

Lisbon ACC100 FEC Accelerator Server Adapter utilizes Intel® vRAN dedicated accelerator ACC100 to provide wire rate forward error correction (FEC) processing while enabling more virtualized functionality on the host server.

5G networks promise high throughput and low latency by design, and one important component of that is having forward error control (FEC) that can ensure wire speed correction of corrupted bits in data messages. The combination of high speed 5G mobile data services and billions of internet of things (IoT) devices sending packets will challenge the FEC architectures that served 4G networks. This demand for high performance FEC is driving the need for a specialized FEC accelerator server adapter card that can deliver the throughput needed for even the fastest networks.

FEC for 5G Networks

The 5G wireless standard is designed for three broadly defined service scenarios: enhanced mobile broadband (eMBB), ultra-reliable and low latency communications (URLLC), and massive machine type communications (mMTC). To support these scenarios, the 5G standard delivers a theoretical maximum bandwidth of 10 Gbps, with latency in the tens of milliseconds and high network efficiency delivering improved reliability.

FEC has long been an important part of ensuring reliable and low latency network throughput. Transmission errors, where bits can be lost, often occur due to noise on the line, interference or low signal strength. The impact of these errors includes reduced throughput, higher latency, poor coverage and reduced quality of service. FEC mechanisms are designed to ensure the corrupted message can be recreated, helping minimize the retransmission of packets, thus reducing the bit error rate of network connections. It does this through a variety of channel coding mechanisms that add redundant information known as parity bits that enable the receiving station to detect and fix bits that are corrupted during transmission.

LDPC for 5G Networks

5G standards bodies have adopted low-density parity check (LDPC) codes as the main FEC mechanism for 5G networks. LDPC was first developed in the early 1960s, but is only now becoming popular because it supports high throughput, a variable code rate and length and hybrid automatic repeat request in addition to good error correcting capability. As shown in Figure 1, a 5G input message is encoded by the LDPC encoder, which adds the parity bits to the original message using a parity check matrix multiplication operation. The message then passes through an additive white gaussian noise channel (AWGN) before being transmitted to its destination, where it is decoded and compared to the input message. It is at this point that block error rates are discovered and the parity bits are used to replace the corrupted data bits and restore the message.
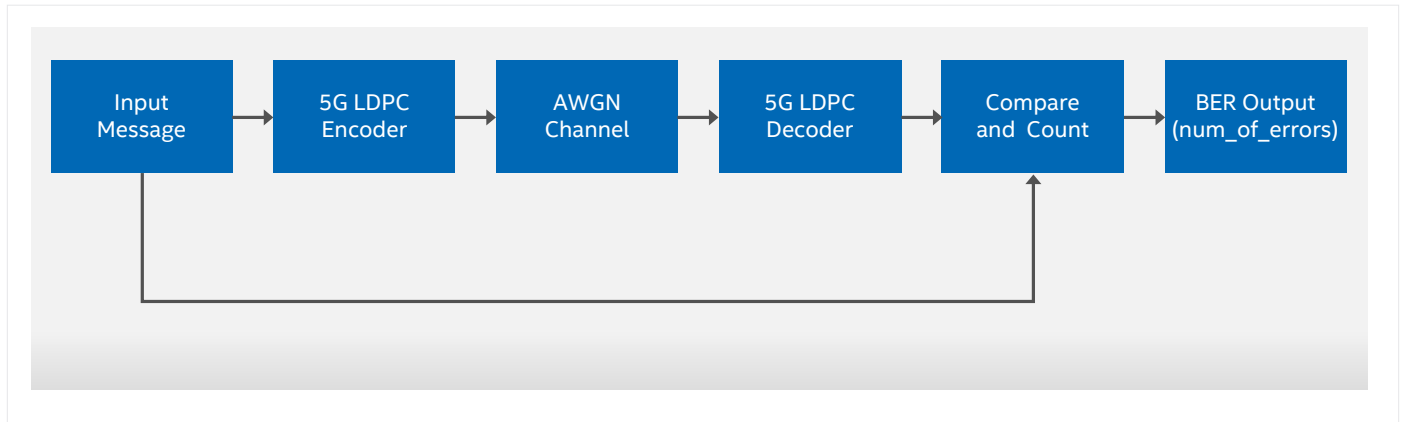
Figure 1. LDPC encoding and decoding process.

FEC in Edge Servers

Another trend affecting performance of the FEC is replacing proprietary baseband systems at the network edge with virtualized/containerized 5G radio access network (vRAN) software running on Intel® architecture-based servers. vRAN systems are compute intensive and must share the CPU's processing cycles with the FEC functionality. This puts pressure on the mobile network operator (MNO) to ensure the server infrastructure is tuned to provide the right resources to both of these applications, and any additional services, such as location services, that need to be deployed on that server.

To deliver high-performance 5G networks, FEC functionality can be accelerated and offloaded from the server host CPU. Intel® Network Builders ecosystem partner Silicom Ltd. has developed the new Lisbon ACC100 FEC Accelerator Server Adapter that utilizes the Intel® vRAN dedicated accelerator ACC100 for performance.

Intel® vRAN dedicated accelerator ACC100 FEC Acceleration Adapter

Silicom's Lisbon ACC100 FEC Accelerator Server Adapter is designed for both 4G (Turbo encoding) and 5G LDPC applications. Some of the adapter's key features include:

- Onboard RAM up to 16GBit DDR4 with ECC

- High throughput x16 PCIe Gen3, X16 Interconnect

- PCI Express Base Specification 3.0 (8 gigatransfers per second)

- Half length, low profile height card dimensions

- Selection of heat sink types optimized to application power / host server limitation

The Lisbon server adapter is designed to be deployed in a range of servers that utilize Intel Xeon Scalable processors. Servers commonly used include rackmount servers with dual-socket Intel Xeon Scalable processors, edge servers with single-socket Intel Xeon Scalable processors, and servers with Intel Xeon D processors.

FEC processing performance in the Lisbon server adapter comes from the Intel vRAN dedicated accelerator ACC100, which features a capacity up to 28 Gbps for high performance data plane or control plane applications. The combination of performance and low power makes it well suited for 5G wireless applications, where it offers a cost-effective, low power solution for accelerating the computing-intensive process of FEC from the host CPU. This frees up more processing power within Intel Xeon processors for channel capacity and edge-based services and applications.
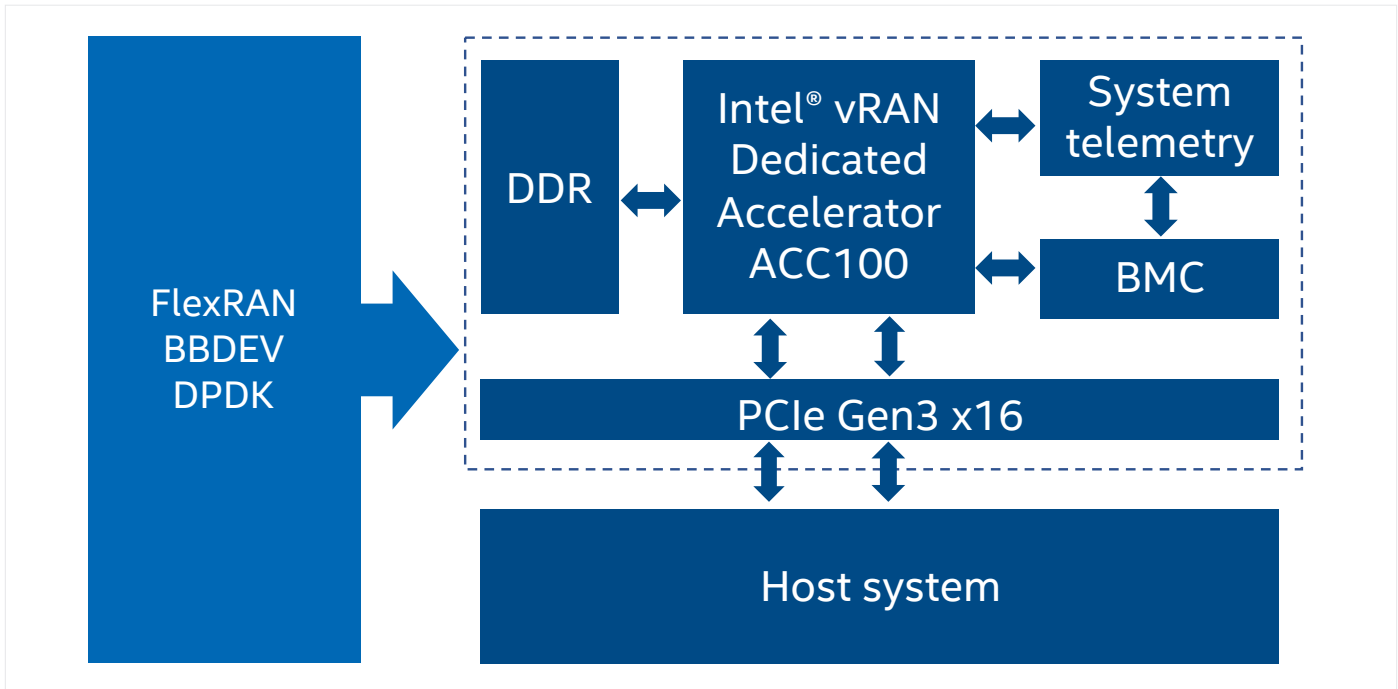
The Intel vRAN dedicated accelerator ACC100 is based on the Intel® eASIC™ N3XS device, a new class of configurable integrated circuit (IC) that balances the fast time-to-market of a field programmable gate array (FPGA) with the power-efficient, purpose-built performance of a custom-developed application specific integrated circuit (ASIC).

The Intel vRAN dedicated accelerator ACC100 on the Lisbon server adapter connects with an external host processor through a x16 PCI Express (PCIe) interface to provide 4G (Turbo) and 5G/LDPC encode and decode functionality. The use of this high-performance bus provides significant performance and non-blocking throughput so that bus performance is not a limiting factor.

The Lisbon ACC100 FEC Accelerator Server Adapter supports hybrid automatic repeat request (HARQ), which augments the FEC capability by enabling high-speed retransmission of data when there are not enough parity bits for FEC to fully restore the corrupted message. The Intel vRAN dedicated accelerator ACC100 is packaged in a 35 mm x 35 mm FC1156 package with 1.0 mm ball pitch (some balls are de-populated to facilitate break-out).

An overview block diagram of the adapter is shown in Figure 2, showing the connections into both the Intel vRAN dedicated accelerator ACC100 and into the software core.

The Lisbon ACC100 FEC Accelerator Server Adapter has a built-in baseboard management controller (BMC) service processor that monitors the physical state of the adapter, including voltage levels, current levels, temperature events and power supplies in order to provide telemetry to the system management module and fault handling to ensure adapter operation, uptime and performance.

Figure 2. Block diagram of the Silicom Lisbon ACC100 FEC Accelerator Server Adapter with the Intel vRAN dedicated accelerator ACC100.

Conclusion

The Lisbon ACC100 FEC Accelerator Server Adapter—part number: P3iMB-M-P1 (standard temp) and P3iMB-M-P2 (extended temp)—is designed to speed up FEC performance in 5G networks to allow this essential network functionality to keep pace with the high data rates expected in 5G networks. Utilizing the Intel vRAN dedicated accelerator ACC100 with its unique combination of high performance and low power along with x16 PCIe interconnect, Silicom is able to process packets in real time to keep up with 5G network performance and fully offload the FEC processing requirement from the host CPU. Working with Intel, Silicom has designed an innovative server adapter that will help deliver the performance and low latency promises of 5G.

Learn More

Silicom USA: https://www.silicom-usa.com

Silicom Lisbon ACC100 FEC Accelerator Server Adapter: https://www.silicom-usa.com/news/lisbon-acc100/

2nd generation Intel® Xeon® Scalable processors: https://www.intel.com/xeonscalable

Intel® eASIC™ devices: https://www.intel.com/easic

Silicom is a member of the Intel® Network Builders ecosystem: https://networkbuilders.intel.com

intel.